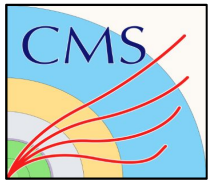
# Tests of the Front-End Electronics for the Phase 1 Upgrade of CMS-HB Calorimeter



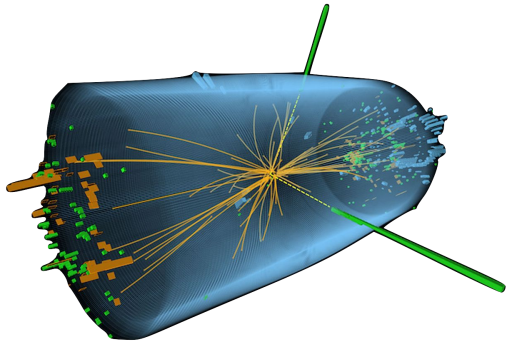
Suat Donertas
January 30, 2020

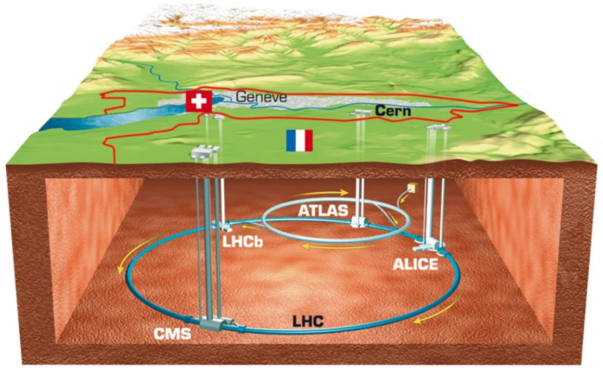
# Outline

- Introduction
  - The Large Hadron Collider (LHC)
  - The Compact Muon Solenoid (CMS)
  - Calorimetry as a Detection Principle
    - The Hadron Calorimeter
    - The Hadron Barrel Calorimeter
- Phase-I Upgrade of the Hadron Barrel Calorimeter (HB)
  - New Generation Clock and Control Module (ngCCM)
- Assembly & Tests
  - Single Board Assembly & Tests
  - Module Assembly & Tests

# Introduction: The Large Hadron Collider

- The LHC is a two-ring superconducting tunnel beneath Franco-Swiss border with a circumference of 27 kms.
- Currently being the most powerful accelerator and collider in the world, the LHC collides two counter rotating beams of protons or heavy ions (Lead) at four interaction points around its ring.
- The LHC accelerates particles up to 0.999999991 times the speed of light and reaches a center of mass collision energy of 13 TeV.



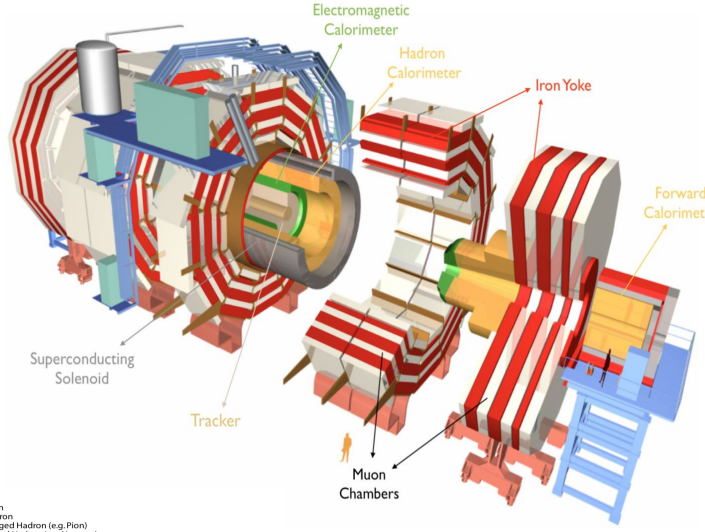


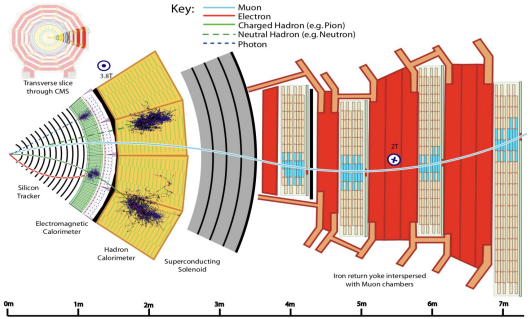

- There are four major experiments located at each one of these four interaction points.

# Introduction: The Compact Muon Solenoid

➢ The Compact Muon Solenoid (CMS) is one of the two multi-purpose detectors of the LHC and it comprises the following sub-detectors/sub-systems:

- Tracker: Measures momentum of charged particles
- Electromagnetic Calorimeter (ECAL): Detects electrons and photons and measures their energy
- Hadron Calorimeter (HCAL): Measures the energy of hadrons
- Muon System: Identifies muons and along with tracker measures muon momentum



# Introduction: Calorimetry as a Detection Principle

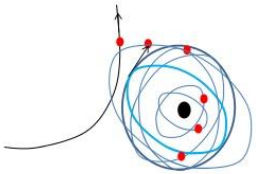
➢ Calorimeter: Blocks of material in which particles get absorbed and their energy gets transformed into a measurable signal either in the form of light or electric charge.

- Homogeneous
- Heterogeneous/Sampling Calorimeters

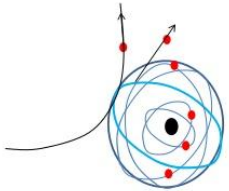
→
- Electromagnetic Calorimeters (could be homogeneous or sampling)
- Hadron Calorimeters (homogeneous is not preferred)

➢ The detection principle mainly relies on ionization and excitation of the calorimeter medium and many more processes like:

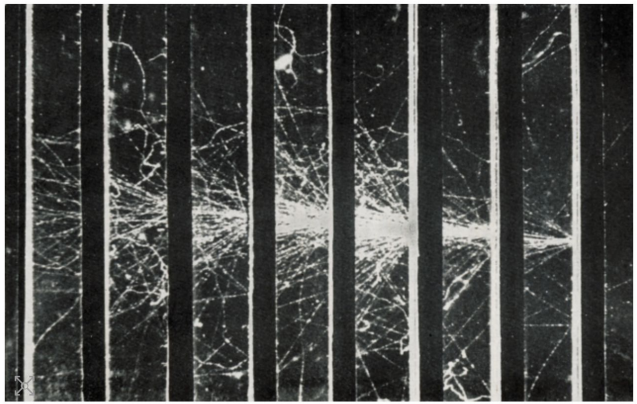
- Bremsstrahlung
- Compton Scattering
- Pair Production
- Cherenkov Radiation
- ...



Excitation



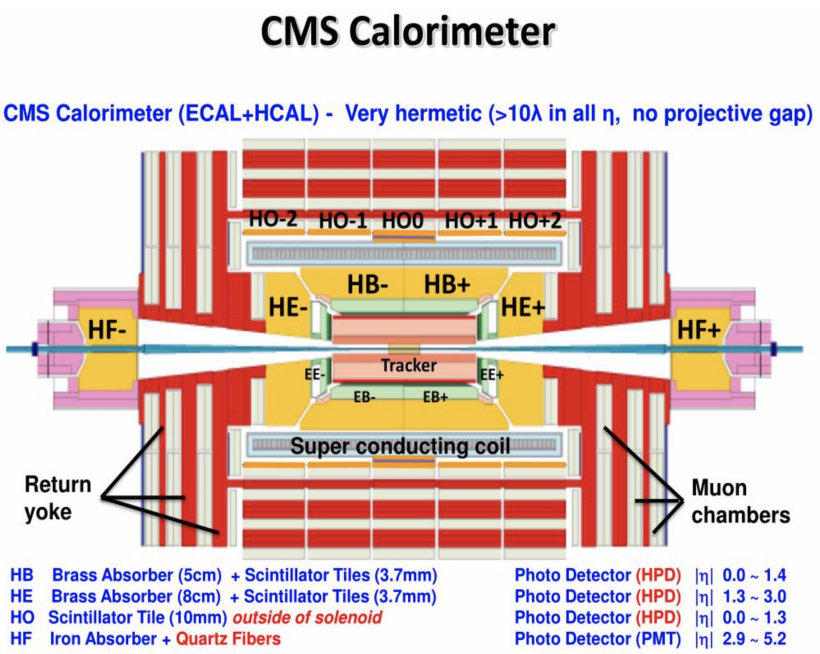
Ionization



Cascade: A shower initiated by a high-energy electron. (Courtesy: C Y Chao, courtesy American Association for the Advancement of Science)

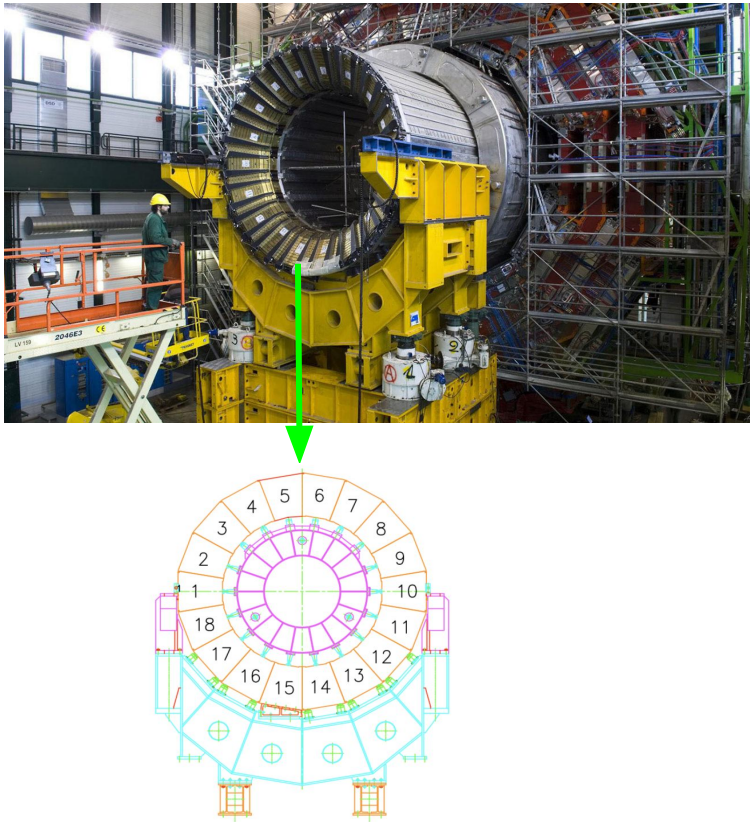
# Introduction: The Compact Muon Solenoid: HCAL

- HCAL is a hermetic sampling calorimeter and is composed of:
  - Hadron Endcap (HE): consists of two disks called HEM & HEP, contributes 2592 readout channels, HPDs as photodetectors
  - Hadron Outer (HO): additional layers of scintillator to measure late starting hadronic showers, consists of 5 rings, contributes 2160 readout channels, HPDs as photodetectors
  - Hadron Forward (HF): cylindrical, contributes 1728 readout channels, PMTs form the readout
  - Hadron Barrel (HB): cylindrically symmetric two half-barrels called HB1 & HB2, contributes 2592 readout channels, HPDs as photodetectors



# Introduction: The Compact Muon Solenoid: HCAL: HB

- The HB calorimeter is a sampling calorimeter consisting of alternating layers of brass absorber and plastic scintillators.
- Consists of 36 wedges, each half barrel having 18.
- The entire readout circuitry is divided into two as Front-End and Back-End Electronics.
- Back End is responsible for the control of readout channels and trigger and timing.
- Front End is responsible for the collection and digitization of collision data and it sits on the detector and is housed in a unit called Readout Box (RBX).

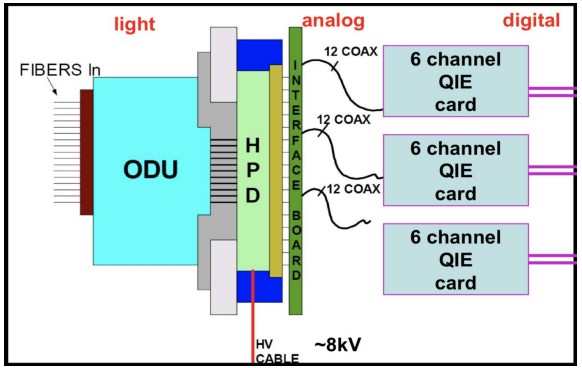


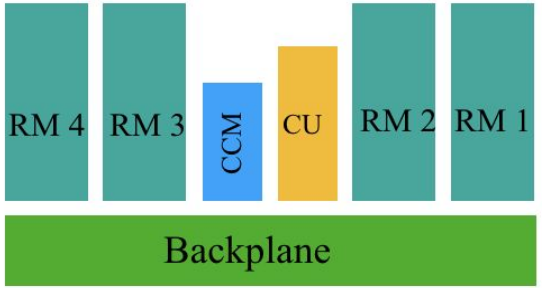
# Introduction: The Compact Muon Solenoid: HCAL: HB

- Readout boxes contain 4 Readout Modules (RM), 1 Calibration Unit (CU), and 1 Clock, Control, and Monitor (CCM) module.

- RMs:
  - The scintillation light collected by WLS fibers are fed into photosensors
  - The charge output from photosensors are then transferred to custom readout cards (QIE) for digitization

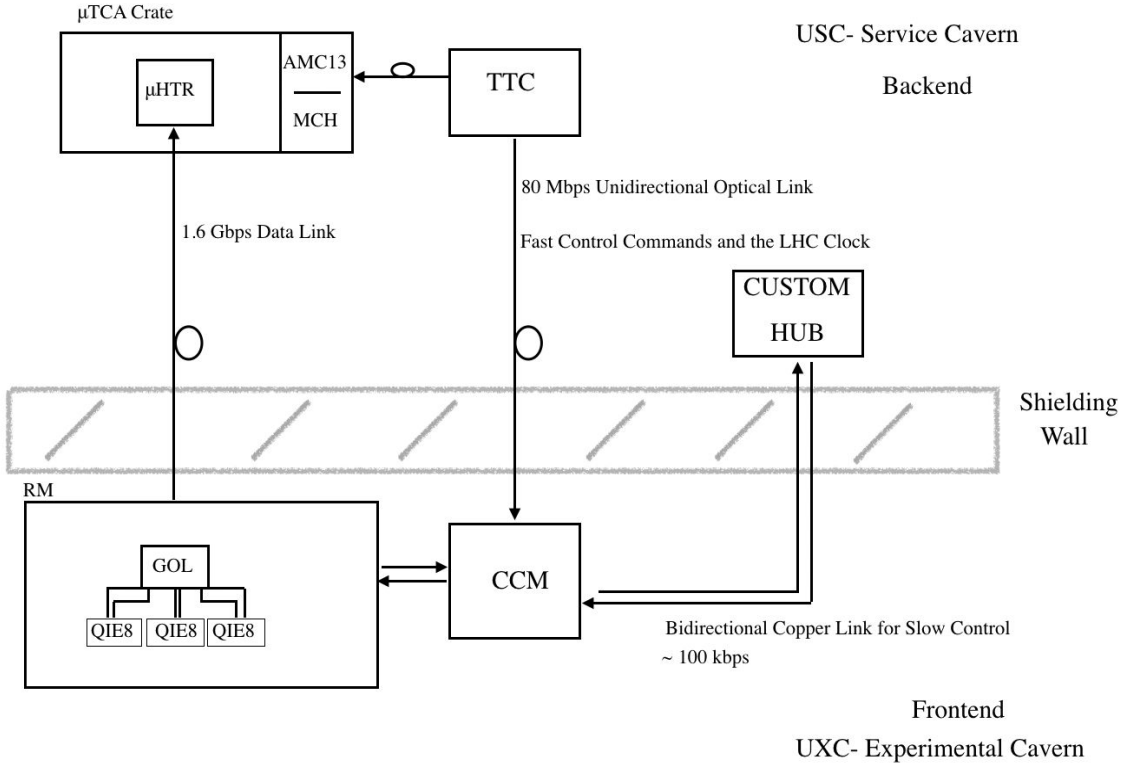
- Clock, Control and Monitor (CCM) module is an important component of the control system by performing:
  - distribution of the LHC clock
  - monitoring of the frontend boards (voltages and temperatures)
  - provide control of the frontend boards for Control System



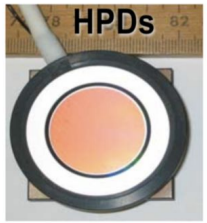

I2C communication between components of an RBX through RBX buses

# Overall Readout & Control Scheme in Phase 0 System



# Phase 1 Upgrade of HB

- The Phase-I Upgrade is the first step of two-staged upgrade plan of the CMS experiment.
- HB specs:
  - Serious radiation damage to scintillators during Phase 0 (required a solution to compensate for the loss in tiles)
  - Phase 0 photodetectors, HPDs, are sensitive to magnetic field and this results in anomalous non-collision signals.



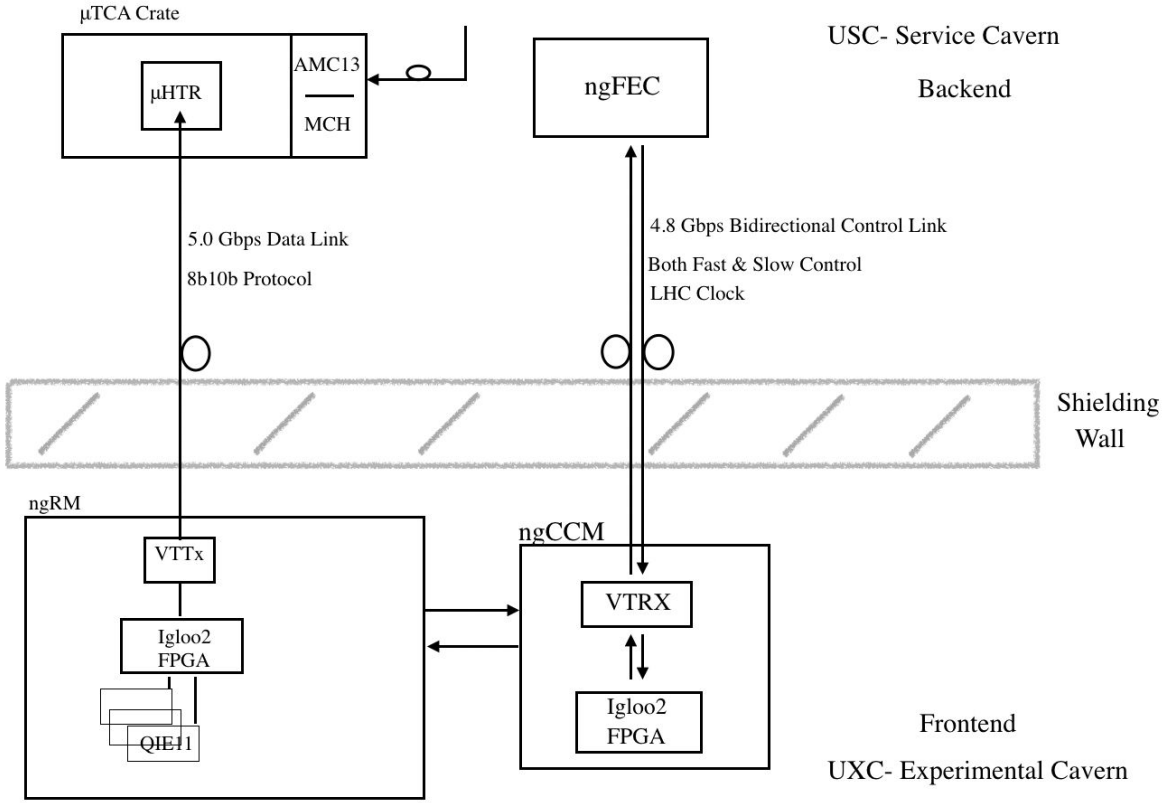

*SiPMs offer way more data channels in the same physical space

- Therefore, the main component of the upgrade is *the replacement of the photodetectors from HPD to SiPM -making it the first large scale use of SiPMs in a radiation environment.*

- CCM design was upgraded with Phase-I requirements in mind and also by keeping the core functions:

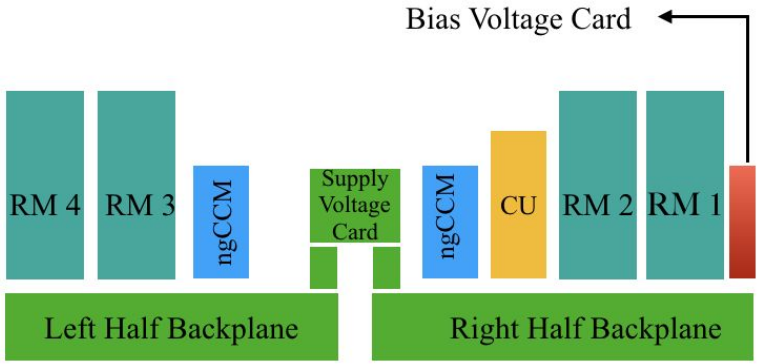
  - needs to introduce a redundancy scheme
  - needs to compensate for the gap in the increased power use
  - needs to upgrade the current ventilation/cooling system
  - needs to be configured to work in tandem with the new faster control link

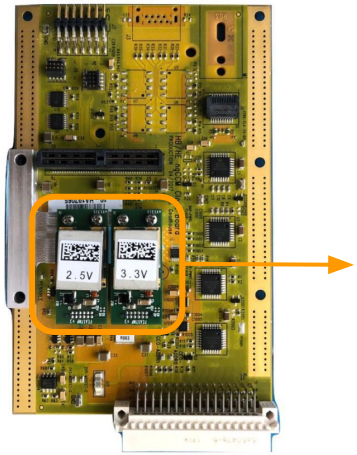
# Overall Readout & Control Scheme in Phase 1 System



# Phase 1 Upgrade of HB: ngCCM

- The redundancy scheme is implemented by splitting the backplane and decreasing the boards per CCM from four to three and increasing the modules per RBX from one to two.

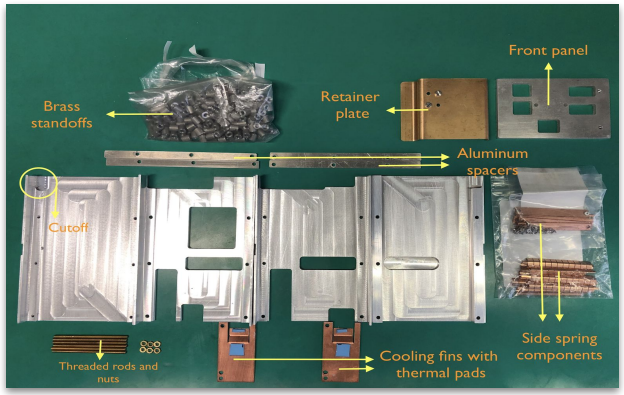


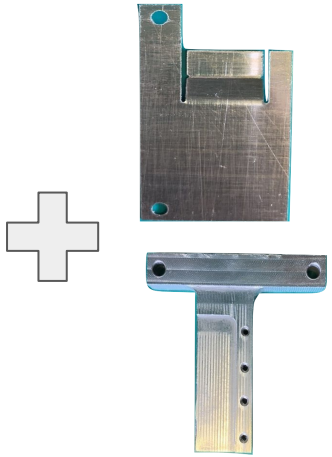



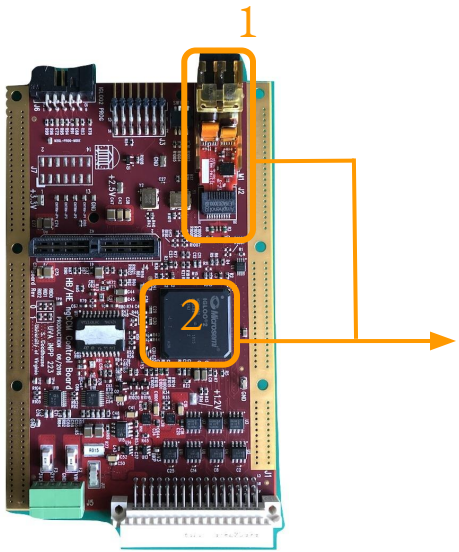

- The DC/DC converters called FEASTMPs were designed at CERN and used to compensate for the gap in power use.

# Phase 1 Upgrade of HB: ngCCM

➢ The current cooling system is upgraded with cooling fins and custom shaped heat sinks for the components with high power consumption (VTRx, FEASTMP).



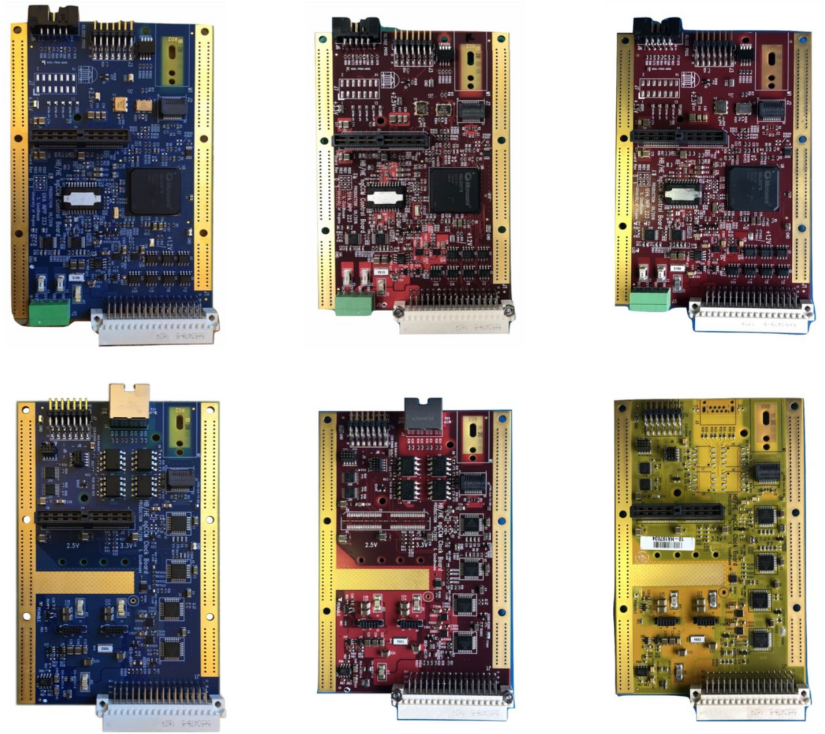



1. Versatile Transceivers (VTRx) are modules designed to work in tandem with GBT.
2. FPGAs programmed with GBT protocol are used to configure the ngCCM with the new control link.

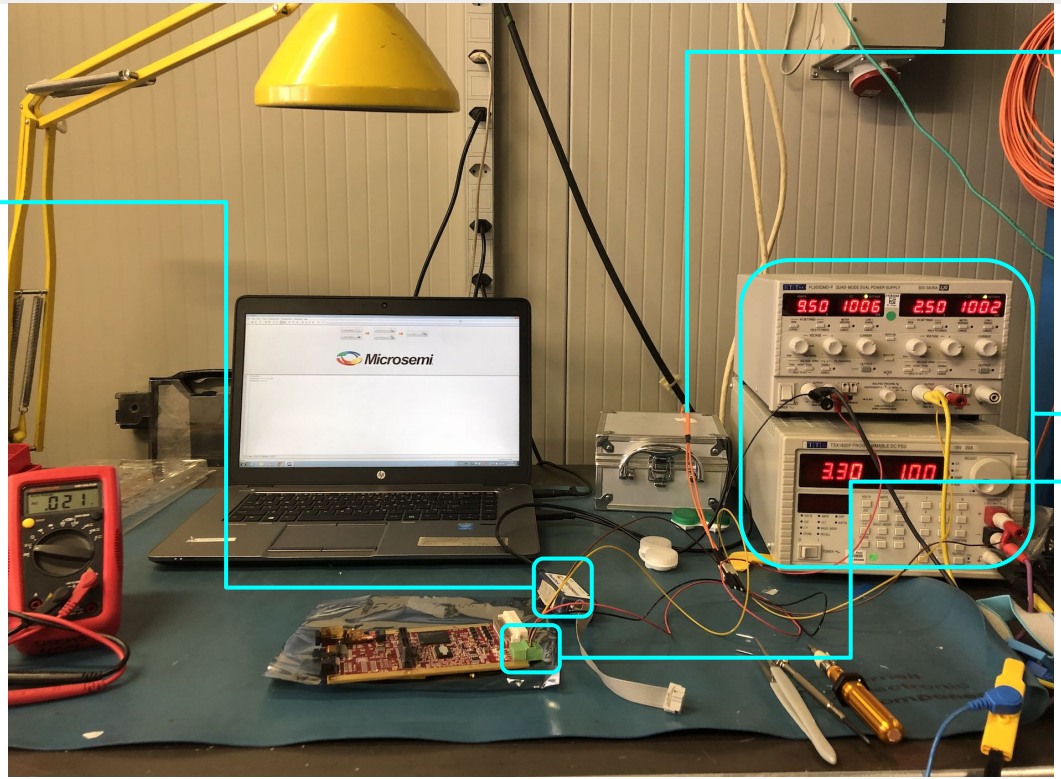
# Phase 1 Upgrade of HB: ngCCM Final Design

- With the upgrade requirements implemented in CCM design, new generation Clock and Control Modules are three-board modules with a simpler design compared to their Phase-0 version.

- Configured as Clock, Master Control, and Slave Control, the three-board design offers a redundant control board, i.e., a redundant control link in case of a corrupted firmware or any other problem that might corrupt the primary link.

# Assembly & Tests: Single Boards - Test Setup



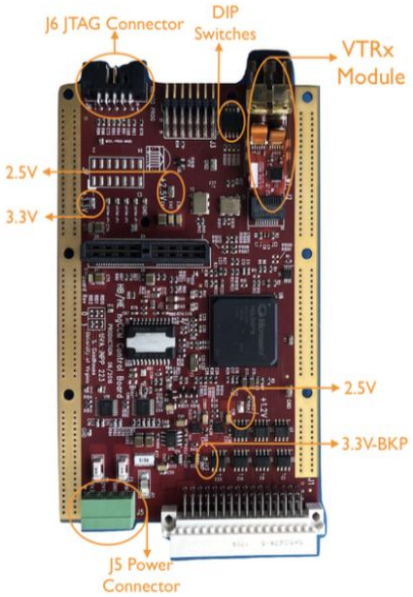

Hardware JTAG programmer

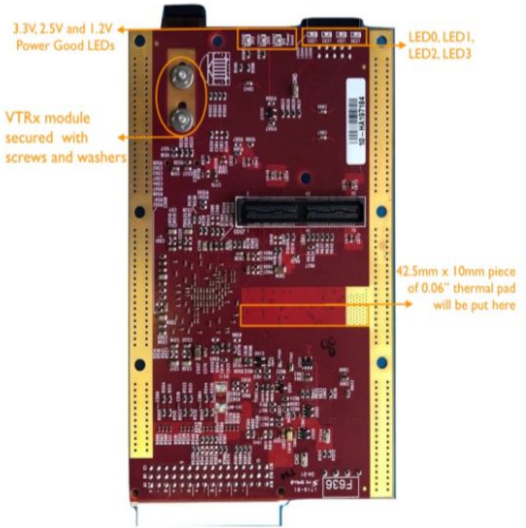
Optical fiber to use the GLIB software

Board is powered via J3 power connector by using three power supplies

# Assembly & Tests: Single Boards - Control Board

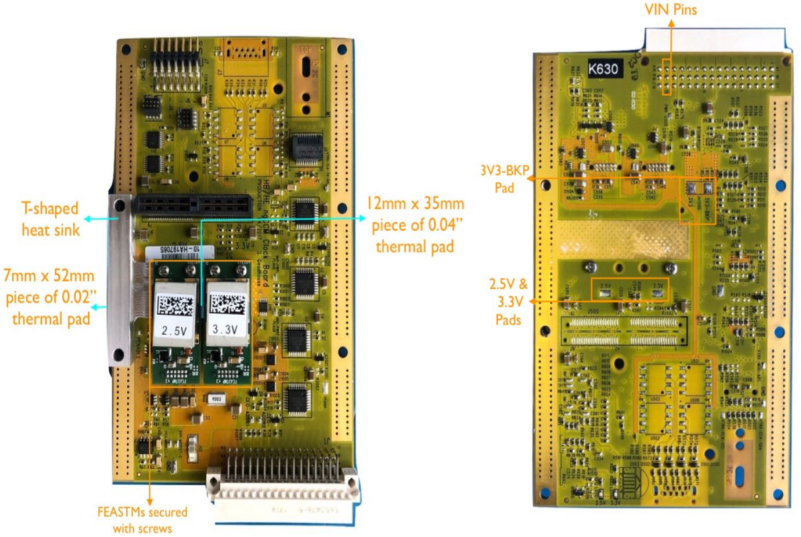
- Visually inspect to detect any manufacturing faults
- Check power supply rails by using the pairwise combinations of 1.2V, 2.5V, 3.3V, 3.3V-BKP, and GND pads to make sure there are no shorts
- Power up the board and read out the currents drawn by each rail
- Check reference clocks' frequencies and voltages
- Program the FPGA and verify programming
- Install a multimode VTRx module
- Check the GBT communication and use ERR_STATUS command to check error counters via GLIBtool
- Use TEMP command to read out the temperatures and temperature IDs via GLIBtool



# Assembly & Tests: Single Boards - Clock Board

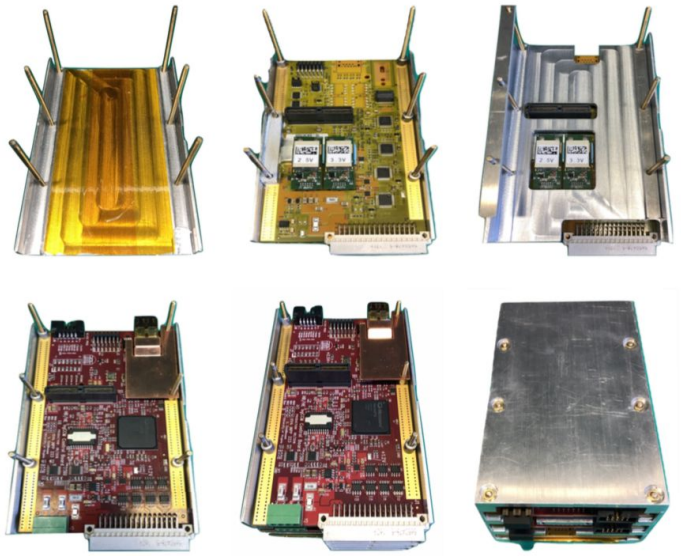
- Visually inspect to detect any manufacturing faults
- Check power supply rails by using the pairwise combinations of 2.5V, 3.3V, 3.3V-BKP, and GND pads to make sure there are no shorts
- Install the custom heat sink complemented with thermal pads and thermal paste and place & secure FEASTMPs on top of it
- Power up the board and measure the voltage output of the two FEASTMPs



## Assembly & Tests: Module Assembly

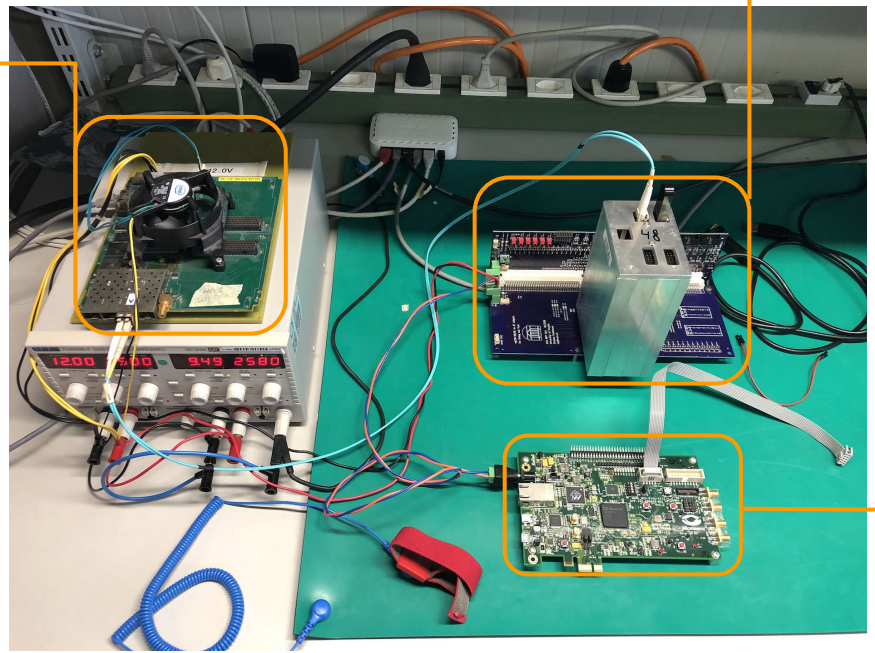
The ngCCMs are housed in aluminum shells of four layers, composing three slots for the three boards.

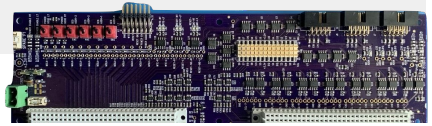
1. The bottom layer is Kapton taped for insulation.
2. Properly tested & assembled clock board is placed through the threaded rods and brass standoffs are placed over them.
3. The second aluminum layer is placed and long aluminum spacers are placed over the rods.

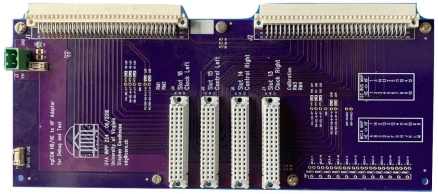


4. The master/primary control board is placed through the rods. Brass standoffs of two different sizes placed over the rods and the cooling fin with thermal pad is placed over the VTRx.
5. Step 4 is repeated for the slave/secondary control board.
6. The top layer is placed and the nuts are tightened on the end of the rods.

# Assembly & Tests: Module Tests - Test Setup

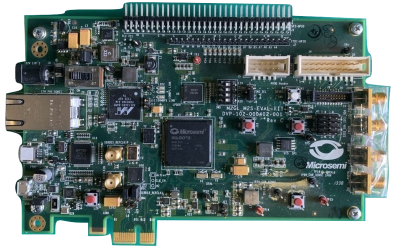






1. Front end emulator board
2. Front end emulator adapter board (the two together as a mock frontend)

- GLIBv2 µTCA board (as a mock control system)



- JTAG evaluation board

## Assembly & Tests: Module Tests

By using GLIBtool software operated in a UNIX environment;

- Check if the communication with GLIBv2 is recovered after repetitive interruptions (GBT Test)
- Check that the power consumption of the ngCCM in a range of voltages is as expected (ADC Check)
- Check that good quality output clocks are received (MCLK Check)
- Check that the input and output signals are transmitted from the ngCCM when told by the GLIBv2 (IO Test)
- Check that the I2C communication is stable (I2C Test)
- Check that the board-to-board communication is stable (B2B Test)
- Check if OneWire Temperature IDs and Temperatures can be read out (TEMP check)
- Check remote programming of FPGAs between the control boards and from the ngCCM to the RMs via JTAG (JTAG Test)

# Assembly & Tests: Module Tests

- GBT Test: checks the error counters for each link between the two control boards and between the GLIB and the ngCCM after the communication link is interrupted.

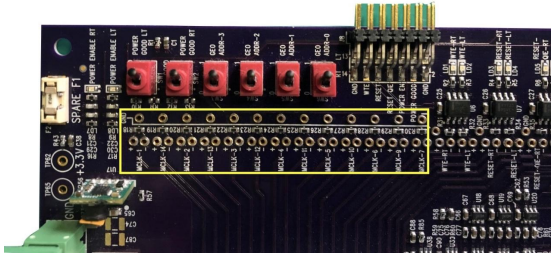
```
Run GBT Test w/ num_iters=10, wait_clear=2, wait_check=10
Can stop GBT test and get summary by pressing Ctrl-C while test is waiting.

  NOTE: Control Link is to J15 with J15 as Master

  NOTE: Direct is using REFCLK1/1 and Neighbor is using REFCLK1/1

1/10 Power Cycling ngCCM with off time=1.50s  .P.W..C..........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:          0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:         0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:     0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:         0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:     0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:         0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:     0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:         0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:     0

So Far:   1 out of   1 PASSED with No Errors after GBT Interruption
```

- ADC Check: verifies the communication and gives the power and temperature readout.

```
HB> adc
  LCLK VIN:  9.32V  IIN:  0.96A  PIN:  8.95W
  LCtl VIN:  9.37V  IIN:  0.03A  PIN:  0.26W
  RCtl VIN:  9.36V  IIN:  0.02A  PIN:  0.21W
  Total Power:  9.42W

       LCLKV  LCLKA   LCtlV  LCtlA   RCtlV  RCtlA   Tot.W
  3V3:  3.31V/ 1.51A   3.31V          3.30V          4.99W
  2V5:  2.51V/ 1.11A   2.50V          2.50V          2.79W
  1V2:                 1.23V/ 0.33A   1.23V/ 0.32A   0.79W
  BKP:  3.27V          3.29V          3.29V
  VTRx RSSI:  0.007mA         0.371mA         0.317mA

  LHC4913 Pwr Diss. 3.3Vin    0.68W           0.66W
  LHC4913 Pwr Diss. 2.5Vin    0.42W           0.40W

  LCLK Temp  U10:  26.25C  U11:  26.25C / LCtl  U18:  30.75C  U19:  29.00C
                                       / RCtl  U18:  30.00C  U19:  27.75C
```

# Assembly & Tests: Module Tests

- MCLK Check: performed with an oscilloscope with active FET probes to verify the quality of master clock delivered by the ngCCM.




- Input-Output (IO) Test: basically checks the backplane inputs and outputs via LEDs and switches on the emulator board.

```
[ HB> io

[  What version of motherboard? (pre-production = 0, production = 1):  [1]
[  Test with both control boards (ENTER=yes, M=master only, Q=quit)

   NOTE: Control Link is to J15 with J15 as Master

[01/28 Test State: Power Enable (lt only)              (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[02/28 Test State: RESET JTAG LEDS                     (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[03/28 Test State: ALL BKP LEDS Off                    (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[04/28 Test State: Power Enable (lt only)              (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[05/28 Test State: Set Power Good LT - switch left     (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[06/28 Test State: Set Power Good RT - switch left     (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[07/28 Test State: Set Power Good LT - switch right    (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[08/28 Test State: Set Power Good RT - switch right    (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[09/28 Test State: Check GEO ADDR all=R                (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[10/28 Test State: WTE (rt & lt)                       (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[11/28 Test State: RESET (rt & lt)                     (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[12/28 Test State: RESET-QIE (rt & lt)                 (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[13/28 Test State: PELTIER-EN-A-LT-N                   (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[14/28 Test State: PELTIER-EN-B-LT-N                   (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[15/28 Test State: ALL BKP LEDS ON (9 LEDs)            (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[16/28 Test State: SEL-ADDR 3/SPR12=000 / CAL-SEL-LT   (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[17/28 Test State: SEL-ADDR 3/SPR12=100 / RM-SEL-A-LT  (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[18/28 Test State: SEL-ADDR 3/SPR12=010 / RM-SEL-B-LT  (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[19/28 Test State: SEL-ADDR 3/SPR12=110 / CAL-SEL-LT   (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[20/28 Test State: SEL-ADDR 3/SPR12=001 / RM-SEL-A-LT  (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[21/28 Test State: SEL-ADDR 012=000 / RM-SEL-A-RT      (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[22/28 Test State: SEL-ADDR 012=100 / RM-SEL-B-RT      (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[23/28 Test State: SEL-ADDR 012=010 / CAL-SEL-RT       (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[24/28 Test State: SEL-ADDR 012=110 / RM-SEL-A-RT      (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[25/28 Test State: SEL-ADDR 012=001 / RM-SEL-B-RT      (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[26/28 Test State: ALL SA LEDS Off / CAL-RT / RM-B-LT  (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[27/28 Test State: ALL SEL-ADDR/SPARE LEDS ON (6 LEDs) (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[28/28 Test State: Power Enable OFF                    (ENTER=proceed, F=prev. fail, S=skip, Q=quit)

 All tested IO reads and writes completed successfully.
```

# Assembly & Tests: Module Tests

- I2C Test: The test goes through all 10 I2C busses and tests reads and writes of I2C. This is done via verifying each slot with 8 test patterns.

```
[ HB> i2c

[ Test all slots (all), half (half) or pick a slot (one) ?  [All]
[  I2C Frequency (Hz):  [80000]

    NOTE: Turning on the backplane power to power the I2C buffers.
    Enabling power on backplane ...

      Backplane PWR-GOOD = 1


   NOTE: Control Link is to J15 with J15 as Master


 NOTE: Data verifies stop with the first data mismatch for each slot/eeprom.

 Testing Pri. Slot: 1 while verifying all slots with each test pattern.

     1: Slot  1  Pri. I2C Addr: 0xA0  expData[0]: 0x00
0000  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0010  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0020  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0030  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0040  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0050  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0060  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0070  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0080  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0090  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00f0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
```

- B2B Test: The main purpose of the test is checking all board-to-board signals by changing the Master/Slave designation of the two control boards J15 and J14.

```
[ HB> b2b


 Test being run while GLIB connected to: J15 (mezz) with J14 (smezz)
 Master is currently J15 and will be restored at the end of the test
 FPGA Version: 05:06

01/18 Test: Normal Mode
02/18 Test: J14 Master mezz  -> smezz
03/18 Test: J14 Master mezz <-  smezz
04/18 Test: J14 Master mezz <-> smezz
05/18 Test: Clear MASTER_J14_ENABLE
06/18 Test: J14 Master mezz <-> smezz
07/18 Test: Reset Mezz  1
08/18 Test: Reset Smezz 1
09/18 Test: J14 Master mezz <-> smezz
10/18 Test: Reset Smezz 2
11/18 Test: Reset Mezz  2
12/18 Test: J14 Master mezz <-> smezz
13/18 Test: Reset Mezz & Smezz 1
14/18 Test: J14 Master mezz  -> smezz
15/18 Test: Reset Mezz & Smezz 2
16/18 Test: J14 Master mezz <-  smezz
17/18 Test: Reset Mezz & Smezz 3
18/18 Test: Return to Normal Mode

All 18 performed B2B tests completed successfully.
```

# Assembly & Tests: Module Tests

- TEMP Check: reads out the OneWire Temperature IDs and ngCCM temperatures.

```
 HB> temp

J14:
     ID #1:  0x289dc8610a00008c   Ur1:  75  Ur2:  70  TEMP:  39.81 C (103.66 F)
J15:
     ID #1:  0x28370f620a0000e4   Ur1:  75  Ur2:  70  TEMP:  40.94 C (105.69 F)
J16:
     ID #1:  0x283ddf610a0000fd   Ur1:  75  Ur2:  70  TEMP:  41.12 C (106.03 F)
```

- After the temperature check, MEZZ_DUMP command is used to dump all known registers inside mezzanine FPGA via I2C (See Backup).

- JTAG Test: consists of six steps and there are two things that are tested. First* is the remote programming of QIE cards in RMs and second** is the remote programming of the ngCCM control boards. (see Backup for a sample output)

  - * is tested in the first four steps by using the evaluation board and by a VERIFY test instead of a full program. In each of these four steps, the evaluation board has a certain blink pattern to its LEDs installed on it which are ignited when a JTAG is successfully initiated.
  - ** is tested in the last two steps by a BYPASS test to make sure overall JTAG protocol is working, instead of a full program. These two steps are to guarantee that in case of a corruption of firmware on any of these control boards, the other can be used to reprogram the corrupted firmware and they are performed without the JTAG evaluation board.

## Summary

- During this assembly & production process, 110 clock & 215 control boards assembled and tested.
  - 4 Clock & 4 control boards failed the tests
- During this assembly & production process, 96 modules built and tested.
  - 3 modules failed the tests
- Three major problems occurred during this process;
  - MCLK signal loss
  - VTRx overheating issue
  - FEASTMP overheating issue
- 92 modules passed all tests and passed onto the burn-in period of 3 weeks.
- After the burn-in period is completed successfully, ngCCMs are going to be installed in the detector by June 2019.

# BACKUP

BACKUP

# Backup

- Backplane signal descriptions for the IO test:

| Output Signal | Description |
|---|---|
| Power Enable: | Enables Backplane Power |
| Power Good: | Signals that FE cards have Good Power Level |
| GEO ADDR: | Selects Geographical Address |
| WTE: | Warning Test Enable for Calibration Purposes |
| RESET: | General Reset |
| RESET-QIE: | Beam Zero |
| PELTIER-EN: | Enables Peltier for SiPMs |
| SEL-ADDR: | Selects JTAG Address |
| CAL-SEL: | Selects Calibration Unit |
| RM-SEL: | Selects Readout Module |

- A sample test output for JTAG test is in the following slide.

```
HB> jtag
  NOTE: Control Link is to J15 with J15 as Master

Select the JTAG Target (PROD1 or EVAL) ?  [EVAL]

01/06 Test PROGRAM   of QIE-RT (via J13/J16) slots 24-27 using J5:

       1. Power off the ngCCM
       2. Verify that the Igloo2 Eval Board (EVB) is powered from the emulator board and its switch is toward the power conn.
       3. Connect "J5" on FE emulator to JTAG conn. on EVB with a ribbon cable.
       4. Power ON the ngCCM and Igloo2 Eval Board (EVB) together.

     Once ready, make your selection (ENTER=proceed, S=skip, Q=quit)

     NOTE: May see some memory corruption errors reported and they can be ignored.
     NOTE: Each JTAG action can take several minutes but a periodic "PERCENT_DONE"
             message will indicate that the action is progressing.

     NOTE: HB Version of ngCCMJTAGSelect()


Jam STAPL Player Version 2.5 (20040526)
Copyright (C) 1997-2004 Altera Corporation

file: "Igloo2_EVB_LEDS_incr1.stp", len: 962726
CRC matched: CRC value = 4D37
Export: key = "JAM_STATEMENT_BUFFER_SIZE", value = 2279
NOTE "CREATOR" = "FlashPro Version: v11.5"
NOTE "CAPTURE" = "11.5.0.26"
NOTE "DEVICE" = "M2GL010T"
NOTE "PACKAGE" = "M2GL010T-fg484"
NOTE "DATE" = "2015/02/12"
NOTE "TIME" = "14:33:41"
NOTE "STAPL_VERSION" = "JESD71"
NOTE "VENDOR" = "Microsemi Corporation"
NOTE "IDCODE" = "0F8031CF"
NOTE "IDMASK" = "0FFFFFFF"
NOTE "DESIGN" = "Igloo2_EVB_LEDS_incr1"
NOTE "DESIGN_DIRECTORY" = ""
NOTE "CHECKSUM" = "2C4B"
NOTE "SECURITY" = "Disable"
NOTE "ALG_VERSION" = "2"
NOTE "MAP_VERSION" = "0"
NOTE "TOOL_VERSION" = "1"
NOTE "MAX_FREQ" = "10000000"
NOTE "SILSIG" = "00000000"
NOTE "SPEED_GRAD" = "-1"
NOTE "TEMP_GRAD" = "COM"
NOTE "PLAYER_VERSION_VARIABLE" = "PLAYERVERSIONVARIABLE"
NOTE "PLAYER_VERSION_SW_VARIABLE" = "PLAYERVERSIONSWVARIABLE"
Frequency: 4000000 Hz
Error: memory corruption detected for allocation #261... bad end guard
Export: key = "ISC_ENABLE_RESULT", 32 bits, value = HEX 00827144
Export: key = "CRCERR: ", 1 bits, value = HEX 0
Export: key = "EDCERR: ", 1 bits, value = HEX 1
TEMPGRADE: ROOM
Export: key = "VPPRANGE: ", 3 bits, value = HEX 7
VPPRANGE: HIGH
Export: key = "TEMP: ", 8 bits, value = HEX 40
Export: key = "VPP: ", 8 bits, value = HEX 61
Programming FPGA Array and eNVM...
Export: key = "PERCENT_DONE", value = 4
Export: key = "PERCENT_DONE", value = 8
Export: key = "PERCENT_DONE", value = 12
Export: key = "PERCENT_DONE", value = 16
Export: key = "PERCENT_DONE", value = 21
Export: key = "PERCENT_DONE", value = 25
Export: key = "PERCENT_DONE", value = 29
Export: key = "PERCENT_DONE", value = 33
Export: key = "PERCENT_DONE", value = 37
Export: key = "PERCENT_DONE", value = 42
Export: key = "PERCENT_DONE", value = 46
Export: key = "PERCENT_DONE", value = 50
Export: key = "PERCENT_DONE", value = 54
Export: key = "PERCENT_DONE", value = 58
Export: key = "PERCENT_DONE", value = 63
Export: key = "PERCENT_DONE", value = 67
Export: key = "PERCENT_DONE", value = 71
Export: key = "PERCENT_DONE", value = 75
Export: key = "PERCENT_DONE", value = 79
Export: key = "PERCENT_DONE", value = 84
Export: key = "PERCENT_DONE", value = 88
Export: key = "PERCENT_DONE", value = 92
Export: key = "PERCENT_DONE", value = 96
Export: key = "Fabric component digest", 256 bits, value = HEX D769881843285B5BAC6FD4D7B9082824854CFA00C9A9783B2EAF2DD729AA9342F
Export: key = "eNVM component digest", 256 bits, value = HEX C2433AFC67C5C5750CF5D7ECC2CF2B0919AE45C6AEBDFA1F10099303712276 5
================================================================================
Export: key = "DSN", 128 bits, value = HEX 03E8AA010000CD5A0023000C001E0022
================================================================================
Error: memory corruption detected for allocation #353... bad end guard
Exit code = 0... Success
Elapsed time = 00:00:50
Memory Usage Info: peak memory usage = 2214193d (2163KB)
Memory Usage Info: peak allocations = 355


     JTAG action "PROGRAM" with "Igloo2_EVB_LEDS_incr1.stp" returned with code: 0

     NOTE: HB Version of ngCCMJTAGSelect()

     Verify that the EVB LEDs show this pattern: Single LED turned ON from right to left (Pass or Fail) pass
```

```
02/06 Test VERIFY    of QIE-RT (via J13/J16) slots 6-9 using J5:

     Once ready, make your selection (ENTER=proceed, S=skip, Q=quit)

     NOTE: May see some memory corruption errors reported and they can be ignored.
     NOTE: Each JTAG action can take several minutes but a periodic "PERCENT_DONE"
             message will indicate that the action is progressing.

     NOTE: HB Version of ngCCMJTAGSelect()


Jam STAPL Player Version 2.5 (20040526)
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file: "Igloo2_EVB_LEDS_incr1.stp", len: 962726
CRC matched: CRC value = 4D37
NOTE "CREATOR" = "FlashPro Version: v11.5"
NOTE "CAPTURE" = "11.5.0.26"
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NOTE "PACKAGE" = "M2GL010T-fg484"
NOTE "DATE" = "2015/02/12"
NOTE "TIME" = "14:33:41"
NOTE "STAPL_VERSION" = "JESD71"
NOTE "VENDOR" = "Microsemi Corporation"
NOTE "IDCODE" = "0F8031CF"
NOTE "IDMASK" = "0FFFFFFF"
NOTE "DESIGN" = "Igloo2_EVB_LEDS_incr1"
NOTE "DESIGN_DIRECTORY" = ""
NOTE "CHECKSUM" = "2C4B"
NOTE "SECURITY" = "Disable"
NOTE "ALG_VERSION" = "2"
NOTE "MAP_VERSION" = "0"
NOTE "TOOL_VERSION" = "1"
NOTE "MAX_FREQ" = "10000000"
NOTE "SILSIG" = "00000000"
NOTE "SPEED_GRAD" = "-1"
NOTE "TEMP_GRAD" = "COM"
NOTE "PLAYER_VERSION_VARIABLE" = "PLAYERVERSIONVARIABLE"
NOTE "PLAYER_VERSION_SW_VARIABLE" = "PLAYERVERSIONSWVARIABLE"
Frequency: 4000000 Hz
Error: memory corruption detected for allocation #261... bad end guard
Export: key = "ISC_ENABLE_RESULT", 32 bits, value = HEX 00826E44
Export: key = "CRCERR: ", 1 bits, value = HEX 0
Export: key = "EDCERR: ", 1 bits, value = HEX 0
TEMPGRADE: ROOM
Export: key = "VPPRANGE: ", 3 bits, value = HEX 7
VPPRANGE: HIGH
Export: key = "TEMP: ", 8 bits, value = HEX 40
Export: key = "VPP: ", 8 bits, value = HEX 61
Verifying FPGA Array and eNVM...
Export: key = "PERCENT_DONE", value = 4
Export: key = "PERCENT_DONE", value = 8
Export: key = "PERCENT_DONE", value = 12
Export: key = "PERCENT_DONE", value = 16
Export: key = "PERCENT_DONE", value = 21
Export: key = "PERCENT_DONE", value = 25
Export: key = "PERCENT_DONE", value = 29
Export: key = "PERCENT_DONE", value = 33
Export: key = "PERCENT_DONE", value = 37
Export: key = "PERCENT_DONE", value = 42
Export: key = "PERCENT_DONE", value = 46
Export: key = "PERCENT_DONE", value = 50
Export: key = "PERCENT_DONE", value = 54
Export: key = "PERCENT_DONE", value = 58
Export: key = "PERCENT_DONE", value = 63
Export: key = "PERCENT_DONE", value = 67
Export: key = "PERCENT_DONE", value = 71
Export: key = "PERCENT_DONE", value = 75
Export: key = "PERCENT_DONE", value = 79
Export: key = "PERCENT_DONE", value = 84
Export: key = "PERCENT_DONE", value = 88
Export: key = "PERCENT_DONE", value = 92
Export: key = "PERCENT_DONE", value = 96
================================================================================
Export: key = "DSN", 128 bits, value = HEX 03E8AA010000CD5A0023000C001E0022
================================================================================
Error: memory corruption detected for allocation #337... bad end guard
Exit code = 0... Success
Elapsed time = 00:00:40
Memory Usage Info: peak memory usage = 2214193d (2163KB)
Memory Usage Info: peak allocations = 355


     JTAG action "VERIFY" with "Igloo2_EVB_LEDS_incr1.stp" returned with code: 0

     NOTE: HB Version of ngCCMJTAGSelect()

     Verify that the EVB LEDs show this pattern: Single LED turned ON from right to left (Pass or Fail) pass
```