FIRMWARE DEVELOPMENT FOR THE FC7 BASED TESTBOARD

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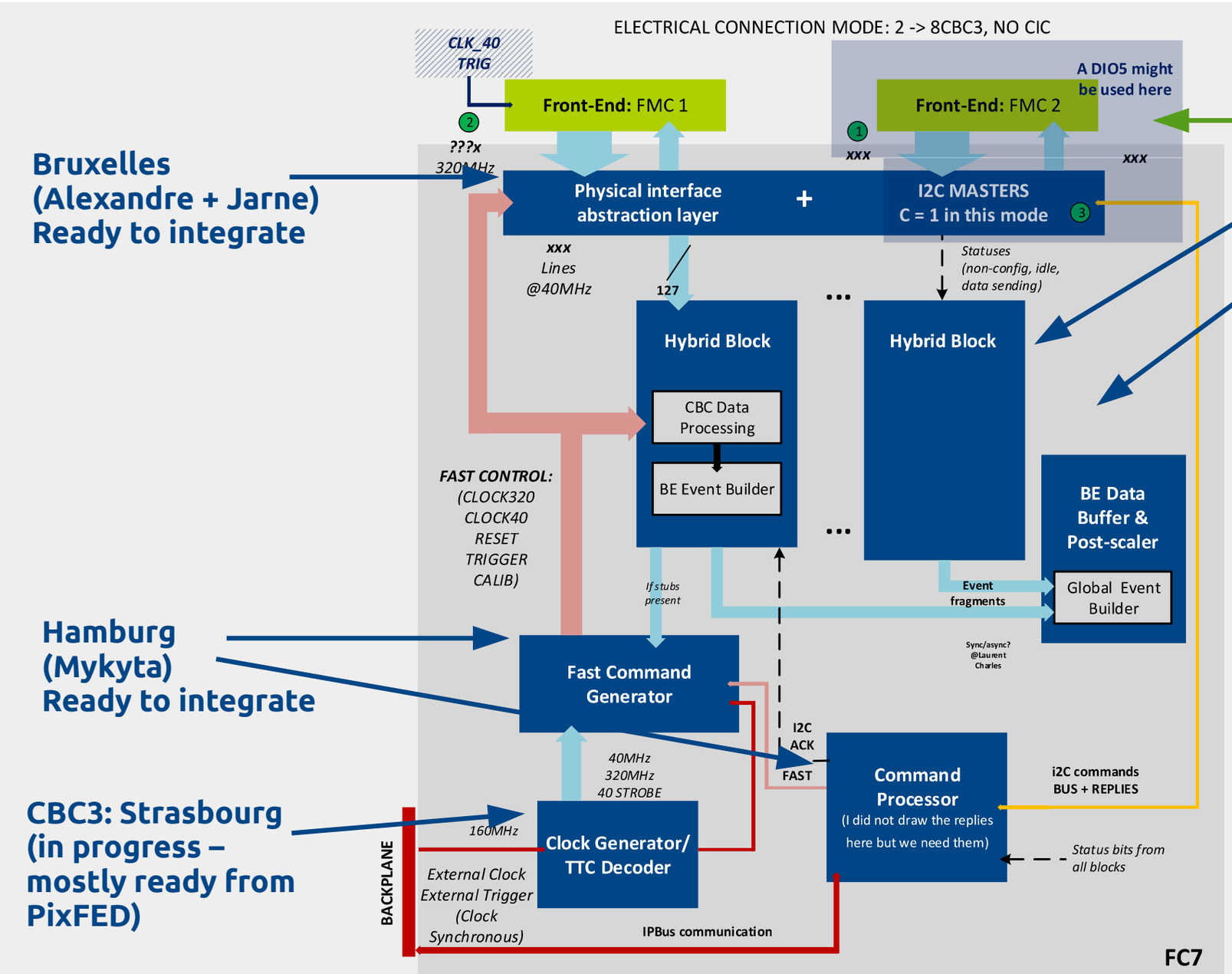
Belgian tracker phase II workshop - 14.03.2017.

BLOCK DEVELOPMENT – D19C



CERN (Mark Kovacs)

MPA+SSA: Rutgers ← on hold
CBC3: Strasbourg (in progress)

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- All urgent items had expression of interest: good starting point
- Actual development can be more fluid if needed, depending on actual work progress
- Implementation started on blocks
- **Proposed goal**: testable version around March?

DAQ meeting – 21 Nov 2016

From S.Mersi

DETECTOR VERSIONS

Dates to be checked / updated with Electronics group. Electronics components described here are considered if part of the connection chain, even if not necessarily integrated on a module.

2×CBC2 — No CIC — Electrical readout **(Present)**
- With GLIB, with legacy FC7 and possibly with d19c (if backwards compatibility)

8×CBC2 — No CIC — Electrical readout **(Present)**
- With GLIB and possibly with d19c (if backwards compatibility – might be very interesting)

2×CBC3 — No CIC — Electrical readout **(April 2017 ?)**
- With d19c

2×CBC3 — No CIC — Optical readout **(~Summer 2017 ?)**
- With d19c

N×(2×MPA) — No CIC — Electrical readout **(~Summer 2017?)**
- With d19c

N×(2×MPA) — No CIC — Electrical readout **(??)**
- With d19c

8×CBC3 — No CIC — Optical readout **(??)**
- With d19c

8×CBC3 — CIC — Optical readout **(??)**
- With d19c

From S.Mersi

FEH

Physical interface layer

Fast command

- forwards the commands to FEH with the proper formatting

Slow control

- receives commands
- decodes
- sends **I2C** to FEH
- sends response back

Stub data readout

- receives stub data from FEH
- formats output to hybrid block

Triggered data readout

- receives triggered data from FEH
- formats output to hybrid block

Fast Command Generator

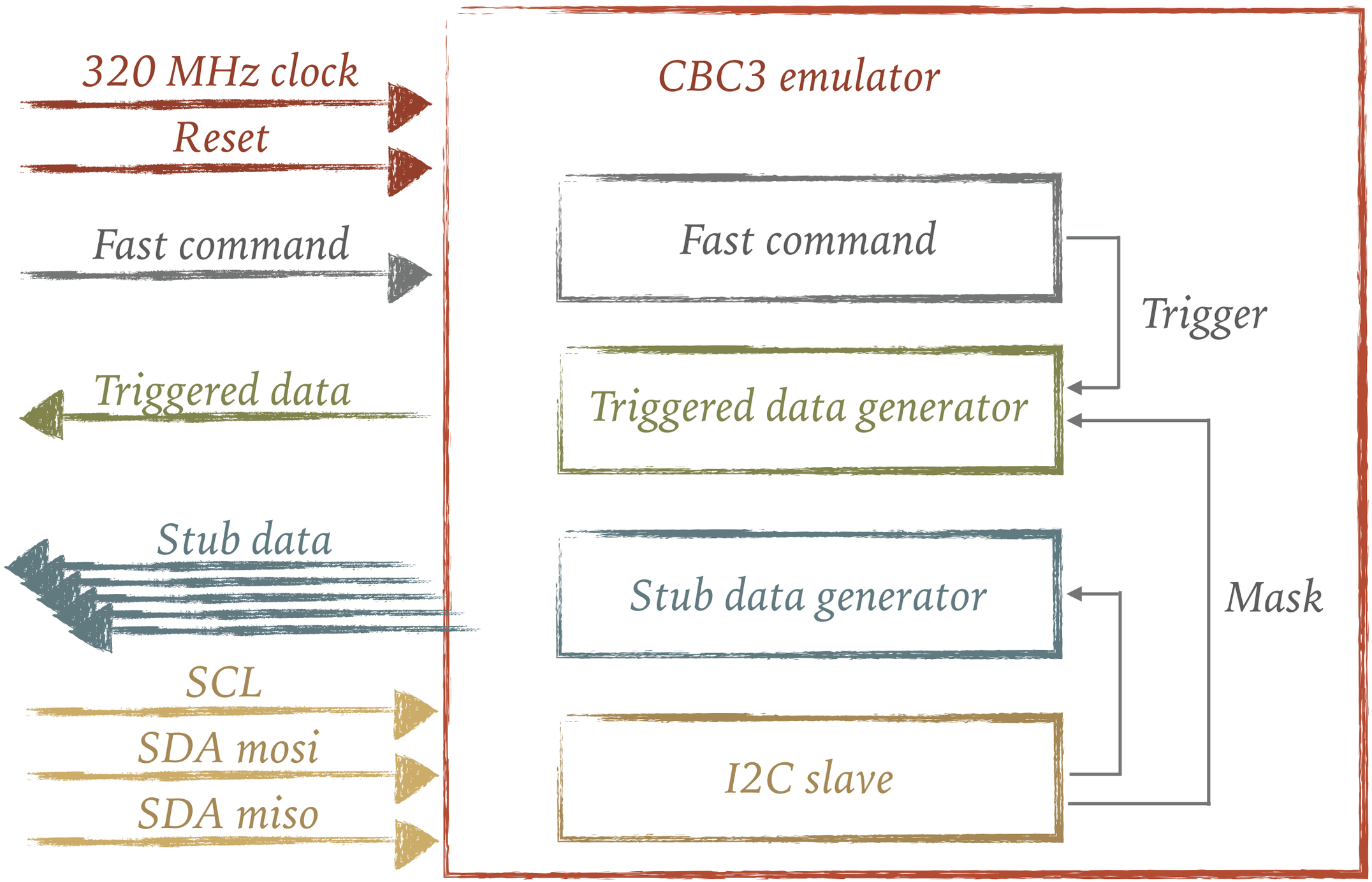
Command Processor

Hybrid Block

CBC3 EMULATOR

- **Basic CBC3 functionality:**
  - Receives fast command sequence
  - Outputs stub data @ 320 MHz
  - Outputs triggered data upon reception of a trigger signal
  - Implemented I2C slave with registers on 2 pages
  - Implemented “channel masking” through I2C mask registers (by default all channels masked)
- Input ports same as for CBC3 chip, except for I2C SDA line
  - no IOBUF, miso and mosi lines directly connected
- Tested with 2CBC3 emulated hybrids

CBC3 EMULATOR



PHY BLOCK CURRENT STATUS

- Code merged with Command generator and Fast command block
- Discovered and resolved some timing issues
- Tested in test bench
- Tested with FPGA using python scripts
- Changed triggered data output as agreed with L. Charles
  - triggered data now goes to hybrid block in 8 consecutive clock cycles
- Ready for first commit

DEVELOPMENT TIMELINE

- **Integration strategy:**
  - FPGA with CBC3 emulator
  - adding backward compatibility with CBC2
- **March:** first firmware integration test
- **June:**
  - Software/firmware integration test
  - beam-test-like configuration
- **Phy block to do list:**
  - Delay lines
  - Implement emulator flag
  - MPA interface

BACKUP

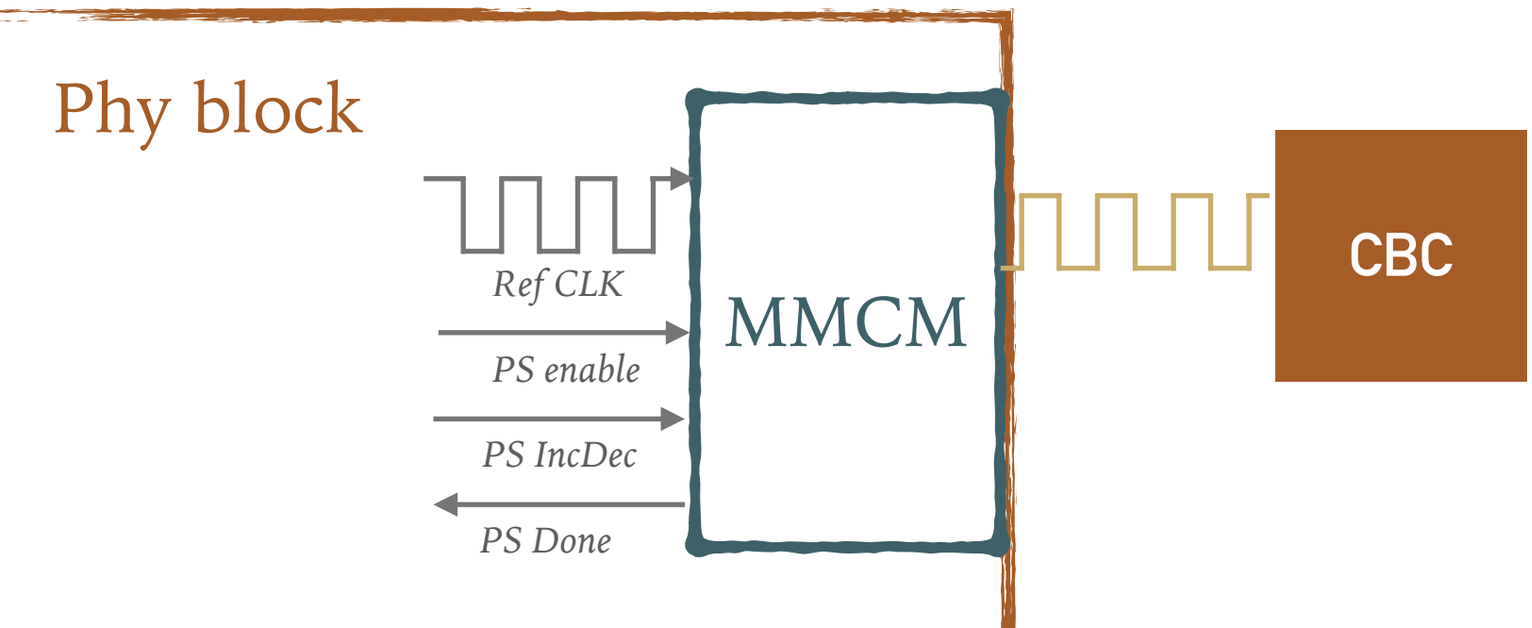
TEST BOARD ON FC7

- A data acquisition card, based on FC7 with electrical or optical connectivity, able to readout 2S or PS (prototype) modules, with or without the CIC
- To support
  - component prototyping and qualifications
  - integration tests
  - beam tests
  - production quality control
- Or dacFC7eo2PwowoCcibpqc in brief
  (if you come up with a better name I'd be happy, otherwise d19c is good enough to me)

From S.Mersi

DELAY LINES

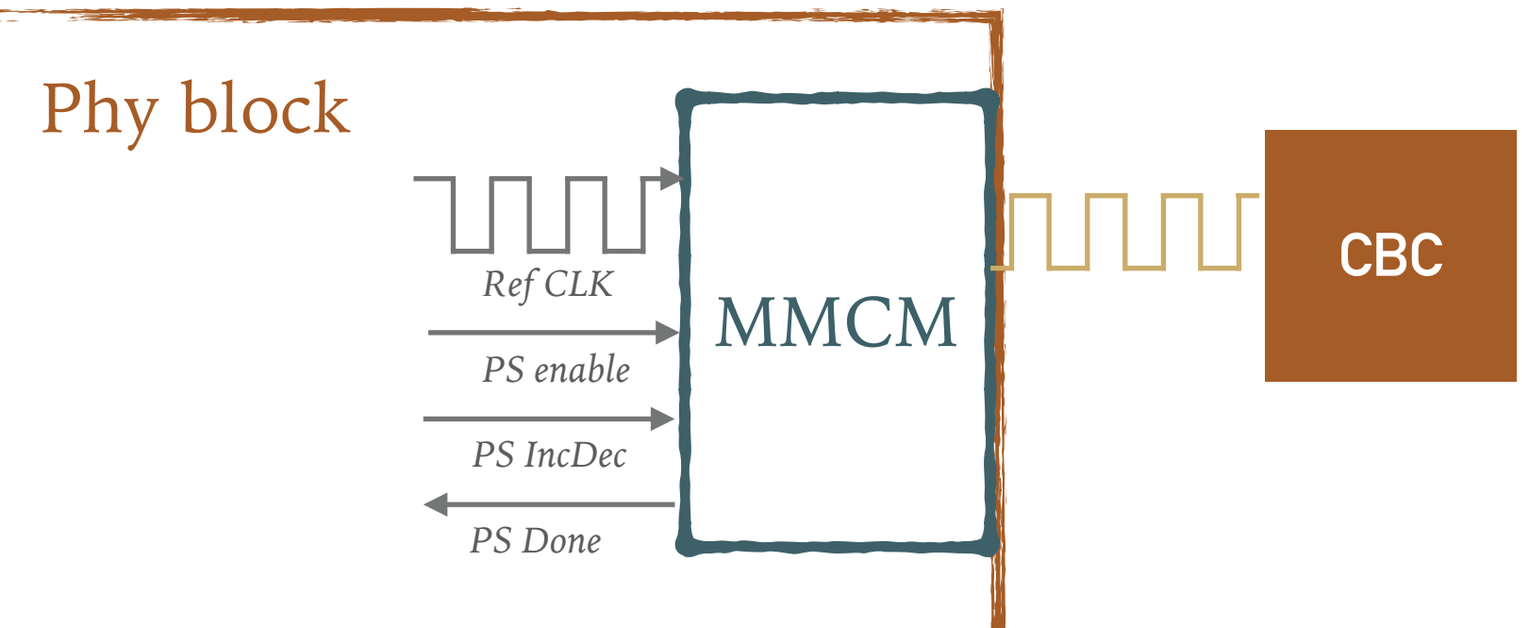
- The idea is to implement delay line to the CBC3 using the MMCM
- Delay the input clock and fast command lines wrt. the “fixed” 320 MHz clock on the FPGA
- Phase shift dynamically determined by looking at the synch bit, still needs to be implemented
- Implementation done per hybrid or per CBC?



DELAY LINES

- Fixed phase shift value of 18.6 ps, no limit on number of consecutive shifts
- It takes 12 clock cycles before MMCM is ready for the next shift
- After the phase shift we will probably need to issue a hard reset to the CBC

- From the discussion with Kirika - not sure what will happen with the CBC if we mess around with the clock



- Investigating also the solution from Kirika

MMCM

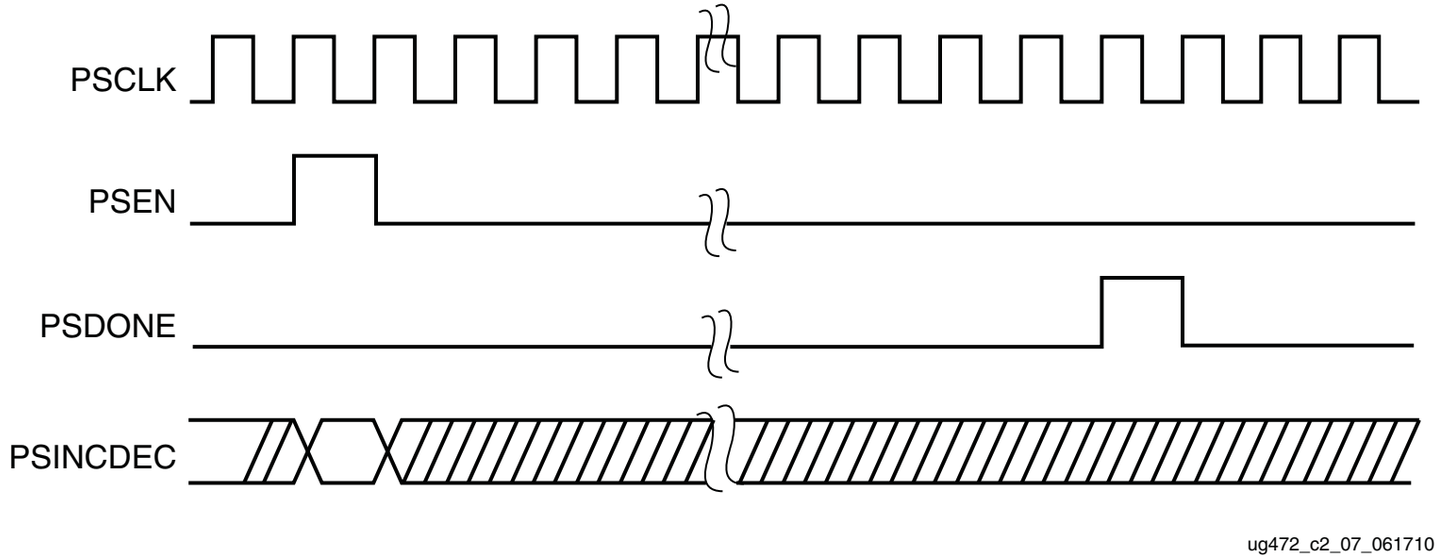


Figure 3-7: **Phase-Shift Timing Diagram**

* *https://www.xilinx.com/support/documentation/user_guides/ug472_7Series_Clocking.pdf*